AN INTEGRATED 18.75/37.5 GHz FET FREQUENCY DOUBLER

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ABSTRACT

The design and performance of an 18.75/37.5 GHz FET frequency doubler is presented. The doubler is implemented in a combination of antipodal finline and suspended microstrip, permitting the entire unit to be integrated on a single substrate. The resulting circuit is a particularly simple and cost-effective component for low and medium power applications such as local oscillators. The doubler was built using a NEC673 FET and has a conversion loss of 5.8 dB over a 350 MHz input bandwidth.

INTRODUCTION

The most important characteristics of the GaAs FET which are exploited for frequency multiplication are the device transconductance and the output conductance. The selection of the bias point determines which of these two characteristics predominates (see Fig. 1). Biasing the FET at Vgs=0, or near pinchoff, gives the most nonlinear operation, enhancing harmonic generation with drain-current clipping. Various studies (2-4) have produced conflicting results as to which is the most efficient mode for frequency doubling: at V_{gs}=0, the device provides greater transconductance, however near pinchoff the increase in input impedance (due to a decrease in gate-source capacitance) results in a larger input voltage swing. The net effect depends on the device characteristics relative to the operating frequencies and power-levels, and must be determined separately for each design, either empirically or with a simulation such as is described in (1).

CIRCUIT DESCRIPTION

The doubler circuit, in Fig. 2, shows the layout of FET mount, bias line, matching stubs plated-through hole choke and finline to microstrip transition. The use of an integrated transition has several advantages, particularly for higher frequency applications: it eliminates the need for complex housings and is reliable and reproducible, resulting in simple, low-cost fabrication. The antipodal finline/microstrip transition used in this design was first described by Van Heuven and results (5,6) indicate that it can provide low transmission loss and good return loss over large bandwidths. The finline taper gradually rotates the E-field by 90 degrees, simultaneously concentrating it into the overlapping region between the two fins (see Fig. 3). At this point, electrical contact with the waveguide wall is no longer necessary, and the resulting balanced, broadside-coupled suspended stripline (BCSS) is transformed to unbalanced microstrip line via a coplanar balun.

A standard small-signal equivalent circuit model for the FET was used in the circuit design. The model element values were derived from the S-parameters of a NEC673 FET mounted in a microstrip test jig and measured from 2 to 20 GHz. The modelled S-parameters were then extrapolated to provide design values at $2f_0$. The matching and bias circuits were realized in microstrip to facilitate tuning. However, the method of mounting the FET on the substrate surface (shown in Fig. 4) requires the use of relatively long, looped bondwires, introducing some uncertainty in the input match.

Preliminary measurements of this device over a range of bias conditions showed that optimum conversion efficiency occurred at V_{gs}=0, and the doubler was accordingly designed to operate at the onset of forward gate conduction, maximizing the conductance nonlinearity. The input was therefore DC-coupled to the waveguide wall via the transition taper, eliminating the gate bias circuit. The drain bias circuit, also implemented in microstrip, was brought out through an insulated gap in the waveguide wall, and included an RC branch in parallel with the open-circuit quarterwave stub. This provided loss at lower frequencies, where the FET was potentially unstable.

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The housing is split-block rectangular waveguide, WR42 at the input and WR22 at the output. The output port is waveguide beyond cutoff at 18.75 GHz, so fundamental rejection is achieved without the need for additional filtering. An abrupt transition from one waveguide dimension to the other occurs in the BCSS portion of the circuit, where the discontinuity has minimal effect on operation.

The circuit is etched on 0.870 x 3.00 x 0.010 inch RT-Duroid (ε_r=2.2) and is clamped in the E-plane of the housing. Plated-through holes are used to maintain continuity in the broadwall of the waveguide and to prevent radiation loss.

DOUBLER PERFORMANCE

The transitions were first measured in a back-to-back configuration. As can be seen in Fig. 5, the resulting loss was about 0.24 dB per transition across the operating range (the WR22 transition showed comparable performance). Some adjustment of the input matching was required to compensate for the effect of the longer bondwires. Tuning was done through a removable section of the housing: the microstrip portion of the circuit was exposed while the finline was left undisturbed so that the overall response was not significantly affected.

The second harmonic output power as a function of input drive level was measured (see Fig. 6) and minimum conversion loss was found to occur at P (f_0) = 12 dBm, where P ($2f_0$) = 6.5 dBm, with a corresponding DC power consumption of 60 mW. The conversion efficiency prior to tuning was about -11 dB, however this was due primarily to insufficient rejection of the fundamental signal by the bias circuit, and was readily improved. The results after tuning are shown in Fig. 7. The conversion loss is 5.8 dB ± 0.15 dB across a 350 MHz input bandwidth, centered about 150 MHz below the design frequency.

CONCLUSION

An integrated FET frequency doubler has been demonstrated in a combination of finline/microstrip techniques. Such an approach exploits the advantages of both media (the ease of analysis and tunability of microstrip and the waveguide compatibility of finline) to produce a simple, low-cost and reliable component suitable for narrow-band millimeter-wave applications in communications and instrumentation.

ACKNOWLEDGMENT

The authors would like to thank Elizabeth Bala for her assistance in circuit fabrication and assembly.

REFERENCES

(1) R. Gilmore, "Design of a Novel FET Frequency Doubler using a Harmonic Balance Algorithm", IEEE 1986 Int. Microwave Symposium Dig., p. 585-588.

(2) C. Rauscher, "High Frequency Doubler Operation of GaAs Field Effect Transistors", IEEE Trans. on Microwave Theory and Technique, Vol. MTT-31, No. 6, pp. 462-473, June 1983.

(3) E. Camargo, R. Soares, R. Perichon, M.Goloubkoff, "Sources of Nonlinearity in GaAs MESFET Frequency Multipliers", IEEE 1983 Int. Microwave Symp. Dig., pp. 343-345.

(4) M. Gupta, R. Laton, T. Lee, "Performance and Design of Microwave FET Harmonic Generators", IEEE Trans. on Microwave Theory and Tech., Vol. MTT-29, No. 3, pp. 261-263, March 1981.

(5) J. Van Heuven, "A New Integrated Waveguide-Microstrip Transition", IEEE Trans. on Microwave Theory and Tech., Vol. MTT-24, No. 3, pp. 144-147, March 1976.

(6) L. Lavedan, "Design of Waveguide-to-Microstrip Transitions Specially Suited to Millimeter-Wave Applications", Electronics Letters, Vol. 13, No. 20, pp. 604-605, September 1977.

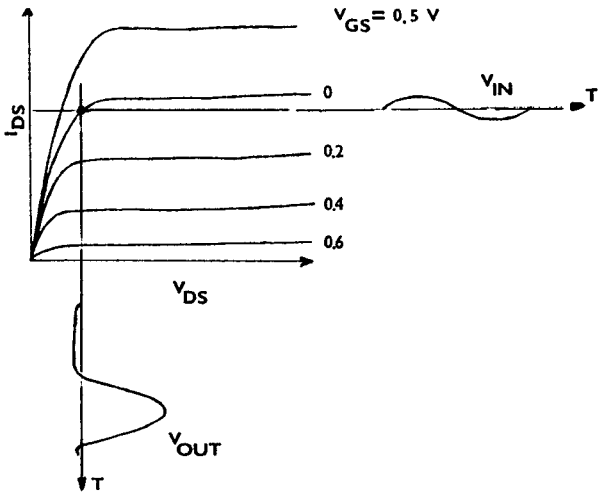

Figure 1a) Gds nonlinearity predominates at Vgs≈0

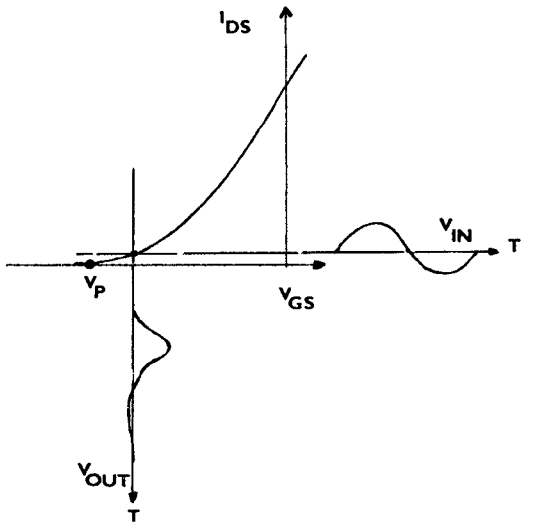

Figure 1b) Gm nonlinearity predominates at Vgs≈Vp

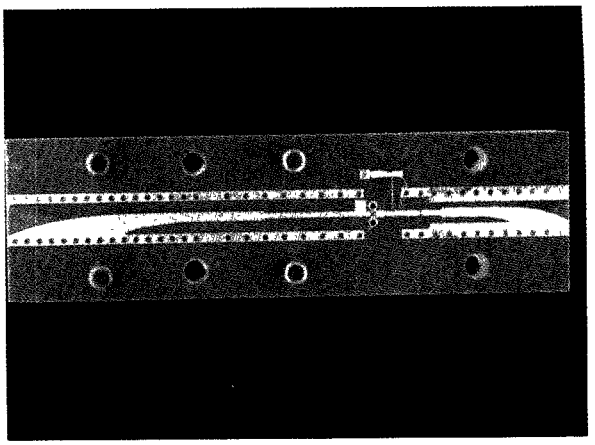

Figure 2) 18.75/37.5 GHz frequency doubler

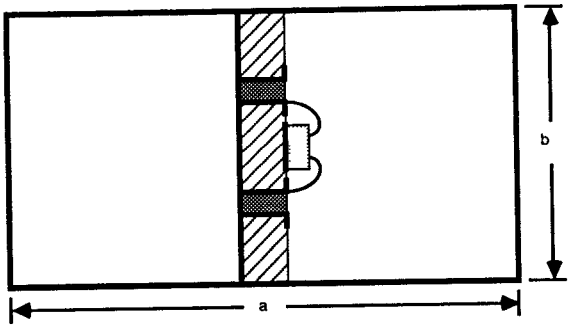

Figure 4) Bonding of source leads to plated-through holes

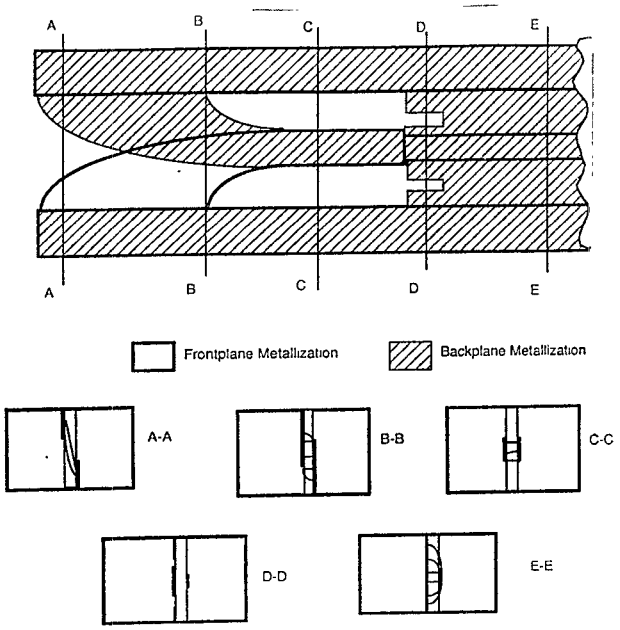

Figure 3) Waveguide-to-Microstrip transition

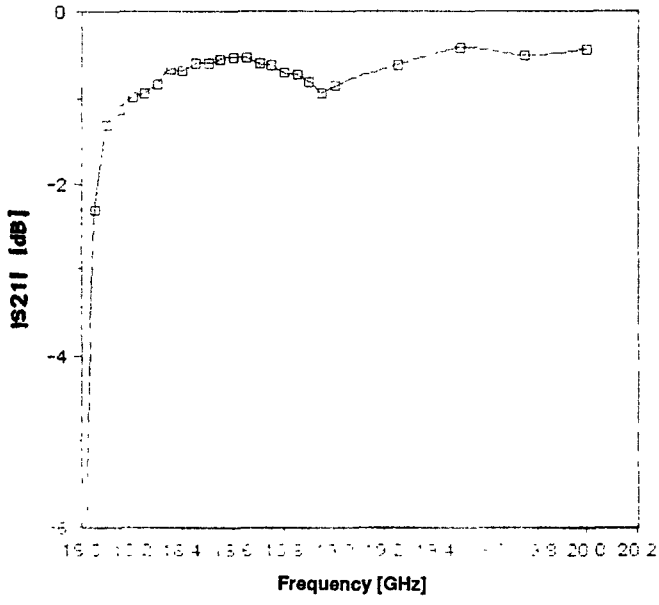

Figure 5) Transmission loss for Back-to-Back WR42 transition

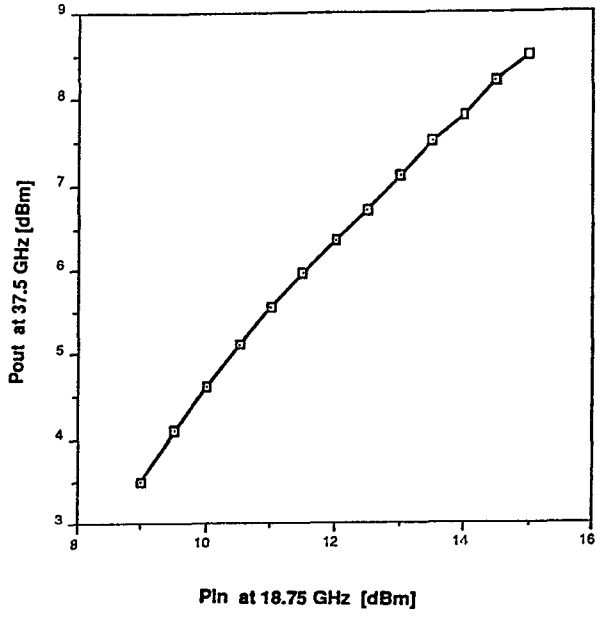

Figure 6) Output power at 37.5GHz for Microstrip/Finline doubler

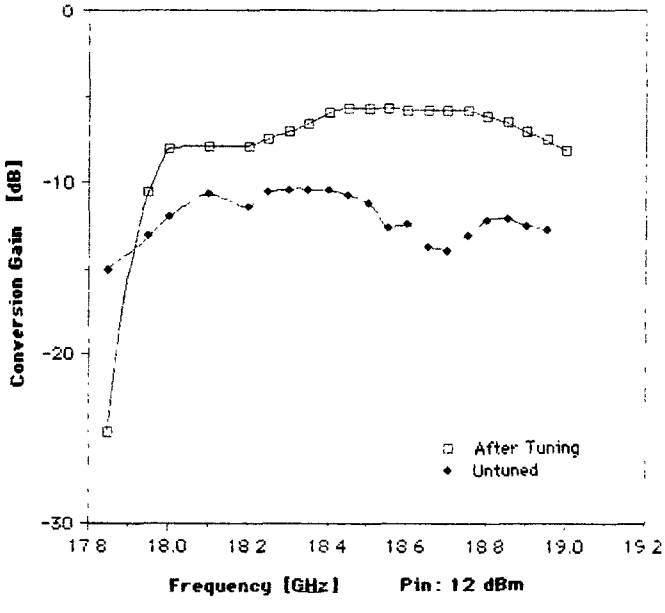

Figure 7) Microstrip/Finline doubler performance